REMARKS

Reconsideration of the present application is respectfully requested. No claims have been amended, canceled or added in this response. No new matter has been added.

Claim Rejections §102

Independent claims 1 and 19 stand rejected under 35 U.S.C. § 102(e) based on Blumenau et al. (hereinafter "Blum", U.S. Patent no. 6,421,711). Applicant respectfully traverses the rejections.

As explained in the response to the previous office action mailed on 11/28/2005. The present invention relates to a virtualization storage server implementing the virtualization functionality using separate storage processors connected by a switching circuit and controlled by a microcontroller so that virtualization can be carried out in hardware by establishing paths between the storage processors. Specifically, Applicant explained in that response that Blum does not teach or suggest the limitation a switching circuit connecting a plurality of storage processors of a storage server, recited in claim 1.

In the present office action mailed on 5/19/2006, the Examiner cites Blum's column 8, lines 3-15, 46-50, 58-65, column 9, lines 44-55, column 10, lines 1-15 and alleges that these sections teach or suggest a switching circuit connecting a plurality of storage processors.

Blum discloses a storage subsystem. As shown in Figure 1 and discussed in column 6, line 64 through column 7, line 9 in Blum, the storage subsystem includes storage volumes (i.e., a plurality of storage disks) and a storage controller. The storage controller has multiple storage adapters and port adapters. Although Blum discloses that each of these adapters may include one or more processors, these adapters are connected by two cache memory busses, not a switching

circuit such as recited in claim 1. By definition, a switching circuit is capable of controlling or routing signals in the circuit to transmit data between specific points in a network. The two busses are just passive electrical signal conduits, not a switching circuit.

Specifically, Blum's column 8, lines 3-15 discloses that the links between the storage adapters and the storage devices may be Fibre Channel fiber-optic loops. That section, however, does not teach or suggest that the two cache memory busses may be Fibre Channel fiber-optic loops. Blum's column 8, lines 46-50 discloses replacing each of the loops 41-44 in Blum's Figure 2 with a switch. As shown in Figure 2, the loops 41-44 are the network 21 connecting all of the hosts. The network 21 is not even part of the cache storage subsystem as shown in Figure 1 of Blum. Thus, Blum's column 8, lines 46-50 does not teach or suggest that the two cache memory busses connecting the plurality of storage adapters and the plurality of port adapters are loops that may be replaced by switches. Regarding Blum's column 8, lines 58-65, the relevant discussion also concerns the network 21, not the two cache memory busses. In addition, Blum's column 9, lines 44-55 and column 10, lines 1-15 all concern the network 21. Thus, none of the Examiner cited sections teaches or suggests that the two cache memory busses may be a switch circuit connecting a plurality of storage processors.

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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